IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): YAMADA et al.	Atty. Dkt.: 1-485
Serial No.: Unknown	Group Art Unit:
Filed: Concurrently herewith	Examiner:
Title: SEMICONDUCTOR INTEGRATED CIRCUIT	

Commissioner for Patents
Arlington, VA 22202

Date: October 8, 2003

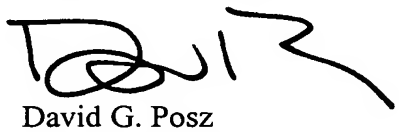
INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, the reference(s) listed on the attached Form PTO-1449 is/are submitted for consideration by the Examiner without any admission that it/they constitute(s) statutory prior art, or without any admission that it/they contain(s) subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

The Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed reference(s) has/have been considered and made of record.

Respectfully submitted,



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FORM PTO-1449	ATTY. DKT NO. 1-485	SER. NO.
	APPLICANT **YAMADA et al.**	
	FILING DATE October 8, 2003	GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

								TRANSLATION YES	TRANSLATION NO
		DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS		
		JP-A-2000-307397*	11/02/00	JAPAN				X (Abstract)	

* Full English text of the JP Document will be available in machine-translated form from JP (Japanese Patent Office) English language web site at **http://www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX**.

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER		DATE CONSIDERED

Rev. 10/94 (Form 3.05)